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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/023,234	02/13/98	HOLMAN	T 042390P5658

TM02/0215
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EXAMINER

VERBRUGGE, K

ART UNIT

PAPER NUMBER

2185

18

DATE MAILED:

02/15/01

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Commissioner of Patents and Trademarks

See attached Examiner's Answer



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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 18

Application Number: 09/023234
Filing Date: 2/13/98
Appellant(s): Thomas J. Holman

Sang Hui Michael Kim
For Appellant

EXAMINER'S ANSWER

Art Unit: 2185

This is in response to appellant's brief on appeal filed 12/21/00.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1-17.

Claims 1, 2, 6, 8, 9, 14, and 17 have been amended subsequent to the final rejection.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

Art Unit: 2185

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

(7) *Grouping of Claims*

The rejection of claims 1-17 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

4,045,781

LEVY ET AL.

8-1977

Art Unit: 2185

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7, 8, 12, and 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claims 1, 2, and 17, Levy shows the claimed memory module as memory module 30 in Fig. 1. Memory module 30 includes the claimed plurality of memory devices as low stack 0-3 and high stack 0-3. Furthermore, memory module 30 includes the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42. This controller receives a first memory transaction in a first format from a first memory bus (memory bus 40) and converts the first memory transaction into a second memory transaction in a second format for the plurality of memory devices as claimed. The second memory

Art Unit: 2185

transaction is clearly different from the first memory format since the outputs of memory transceiver 41 and memory control and timing unit 42 are clearly different from their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures (specifically Fig. 11, which details memory control and timing unit 42) and the disclosure (specifically column 6, line 1 through column 9, line 68 and column 16, line 1 through column 17, line 44).

Regarding claim 3, Levy shows the claimed second memory bus as the signal lines coming out of memory transceiver 41 and memory control and timing unit 42.

Regarding claim 4, Levy's second memory bus includes the claimed address, data, and control signal lines as shown in Fig. 1.

Regarding claim 5, Levy's second memory bus includes the claimed signal line for a clock signal (timing signal) as shown in Fig. 1.

Regarding claim 7, Levy's memory buses clearly have different numbers of signal lines as shown by Fig. 1.

Art Unit: 2185

Regarding claim 8, Levy shows the claimed request handling circuitry as memory transceiver 41 and shows the claimed control logic as memory control and timing unit 42.

Regarding claim 12, Levy teaches that his memory devices are volatile, as claimed, since they are traditional random access memory devices.

Regarding claim 14, Levy does not explicitly mention the claimed handshake signal, however it is inherent in his device since his memory controller necessarily communicates data to the system memory controller (memory management unit 22). It is clear that the memory module controller communicates data and control signals to the system memory controller since the data (D) and control (C) lines of memory bus 40 are bidirectional.

Regarding claims 15 and 16, Levy teaches that his device performs the claimed reads and writes.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a

Art Unit: 2185

person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6, 9, 10, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claim 6, Levy does not teach that his memory buses operate at different rates, however it would have been obvious to one skilled in the art at the time of the invention to operate them at different rates since they carry different signals and have different lengths, virtually ensuring that the maximum data rate of each one would be different.

Regarding claim 9, Levy shows separate address and data lines for both his first and second memory buses. He does not teach that his first memory bus carries time-multiplexed data and address information as claimed, however it would have been obvious to one skilled in the art to time-multiplex the first address bus to save signal lines and their associated cost and space.

Regarding claims 10, 11, and 13, Levy does not teach that his memory modules have the claimed characteristics, however it would have been obvious to the skilled artisan at the time of the invention to implement Levy's memory modules as SIMMs, DIMMs, or

Art Unit: 2185

nonvolatile memory devices, as appropriate, depending on design considerations, since all three types of devices were well-known to the artisan.

(11) Response to Argument

Appellant's only argument is essentially that Levy fails to show a memory module controller that receives a first memory transaction in a first format and converts it into a second (different) memory transaction in a second (different) format for the plurality of memory devices to which the memory module controller is connected.

Levy clearly shows the claimed memory module controller as memory transceiver 41 and memory control and timing 42 in Fig. 1. The only dispute is whether this memory module controller converts a received first memory transaction having a first format into a second memory transaction having a different format.

Appellant argues that "memory control and timing circuit 42 initiates a memory cycle after receiving BYTE MASK and ADDRESS PARITY signals. As such, the memory and control timing circuit of [sic] 42 of Levy does not teach converting a first memory transaction into a second memory transaction as recited in claim 1" (emphasis preserved, Appellant's Brief, page 9, first full paragraph). This is Appellant's only support for Appellant's only argument.

As an initial matter, it is noted from Fig. 1 that the memory management unit 22 transmits address (A), data (D), and control (C) signals through associative memory 24, onto

Art Unit: 2185

memory bus 40, and to the memory module controller (memory transceiver 41 and memory control and timing unit 42). From the figure, it is clear that some reformatting of the data occurs in memory transceiver 41 since the data output from memory transceiver 41 is split onto a low bus for low stacks 0-3 and a high bus for high stacks 3-0. Since the figure indicates parallel operation occurs between similarly numbered low and high stacks, it appears that incoming data is reformatted or split and half is stored in a given low stack, and half is stored in a corresponding high stack.

Furthermore, the outputs from memory control and timing unit 42 indicate that some reformatting is taking place therein: a data gating control signal is transmitted to the memory transceiver 41 and various control and timing signals are output from the memory control and timing unit 42 to each low stack unit and each high stack unit (each memory device).

The fact that the first memory transaction (output by memory management unit 22) has a first format and the second memory transaction (output by the memory module controller comprising the memory transceiver 41 and memory control and timing unit 42) has a different format is further evidenced by the figures which detail the separate units. Fig. 6 is a block diagram of the memory management unit 22 and shows the various signals output from memory management unit 22. Fig. 20 is a diagram of a portion of memory transceiver 41. Fig. 11 is a diagram of memory control and timing unit 42. Simple inspection of these figures, especially Fig. 11 and its associated Figs. 12-17, indicates that the memory transaction received by memory transceiver 41 and memory control and timing unit 42 is not merely

Art Unit: 2185

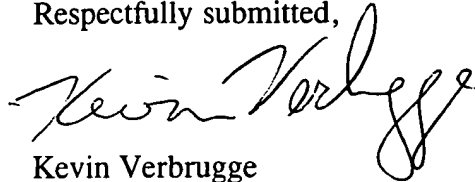
passed on to the memory stack devices but is reformatted to meet the intricate timing and control requirements of the individual low and high stack elements.

Levy further discloses the operation of the circuitry shown in the figures in the disclosure, specifically at column 6, line 1 through column 9, line 68 and column 16, line 1 through column 17, line 44. A careful reading of the disclosure reveals that memory control and timing unit 42 does not merely receive BYTE MASK and ADDRESS PARITY signals as asserted by Appellant, but rather that memory transceiver 41 and memory control and timing unit 42 receive a memory transaction in a first format and convert it into a series of address, data, timing, and control signals to control the operation of the memory devices (low stack 0-3 and high stack 3-0).

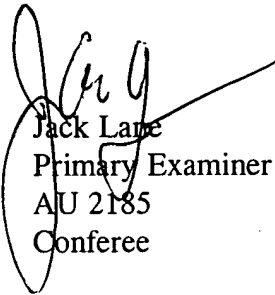
Art Unit: 2185

For the above reasons, it is believed that the rejections should be sustained.

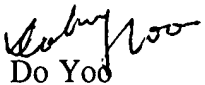
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February 13, 2001

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